Ocean Color Experiment Ver. 3 (OCE3)

~ Concept Presentations~

Electrical

June 18, 2011

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Agenda

- Introduction Electrical Subsystem
- Subsystem Requirements and Assumptions
  - SWIR channels
  - CCDs
- Design Summary
  - Mass, power, volume, data rate materials
- List alternatives to your subsystem not considered or discarded (and why)
- Discuss lead time for any long lead components in your subsystem
- Risks/Concerns
- Conclusion
- Future Recommendations for the very next steps for the customer team to take in their instrument development

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Requirements/Assumptions

- Requirement: 69 SWIR channels
- Requirement: 1 km red chip, 2 taps per 6 channel readout = 12 channels
- Requirement: 1 km blue chip, 2 taps per 6 channel readout = 12 channels
- Requirement: 1 250m visible chip, 2 taps per 12 channel readout = 24 channels

- Assumption: solar calibration, set a bit based on door mechanism, don't collect data
- Assumption: not taking data on un-illuminated portion of scan drum, set a bit

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Scope of Work / Major Drivers to Electrical

1. **Incorporate 3 CCD detectors to the electrical architecture and thermal model**
   - 1km Blue CCD, 1km Red CCD, 250m Visible CCD
2. **Reduce fiber channels to 69 channels.**

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Study Action Affecting Electrical Subsystem

1. Ground coverage and integration periods
2. CCD formats and operating temperature requirements/stability
3. NIR and SWIR channel SNR requirements (this may confirm detector operating temperature)
4. CCD detector readout scheme because of how data is aggregated

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Continuous Scanning Parameters and Data Rate

- **Continuous Scanning Parameters and Data Rate**

700 km Altitude translates to 6.76 km/s ground speed

1 full scan (360 degrees rotation), 3.0 km ground translation per scan

0.44 sec / scan

scan assembly rate: 2.25 Hz / 135 rpm

5098 samples at 1 km intervals per 360 degree rotation

(87.05 μs /sample)

+/- 51 degree imaging sector, 1473 samples at 1 km per scan

20,395 samples at 250 m per 360 degree rotation

(21.76 μs/sample)

+/- 51 degree imaging sector, 5892 samples at 250 m per scan

- **Instantaneous (Peak) Data Rate:**

1 km spectrometer data: 96 X (1 sample / 87.05 μs) X 6 slits X 14 bit = 92.64 Mbit/s

250 m prism data: 96 X (1 sample / 21.76 μs) X 12 slits X 14 bit = 741.18 Mbit/s

1 km fiber data: 7 X 3 X (1 sample/87.05 μs) X 14 bit = 3.38 Mbit/s

250 m fiber data: 4 X 12 X (1 sample / 21.76 μs) X 14 bit = 30.88 Mbit/s

Total = 868.7 Mbit/sec raw uncompressed

After compression (2:1) = 434.35 Mbit/s

With CCSDS Overhead (1.02) = **443.0 Mbit/s**

Peak Data Rate = 443.0 Mbit/s

Average Data Rate = (102/360) (443.0 Mbit/s) = 125.5 Mbit/s

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Integration Period, Taps, ADC Frequency

$SP\_1km = 16$

$\tau\_iFOV = 87.04704 \times \mu s$

$SP\_250m = 4$

$\tau\_250m := \frac{\tau\_iFOV}{SP\_250m} = 21.76176 \times \mu s$

$Bands_G = 45$

$Bands_P = 90$

A/D Conversion rate

$$AD\_Tap\_freq(SP, \tau, Bands) := \frac{SP \times Bands}{\tau \times Taps}$$

$AD\_Tap\_freq(SP\_1km, \tau\_iFOV, Bands_G) = 4.13569\,MHz$

$AD\_Tap\_freq(SP\_250m, \tau\_250m, Bands_P) = 8.27139\,MHz$

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Preamps for Photodiodes

- **Preamps reside near the detectors with the detector electronics**
- **Although Pre-amp board configuration has changed to accommodate detectors,**
  - The number of electrical signals coming to the digitizer electronics is the same

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Design Drivers that Influenced Baseline

- **CCD Drivers**
  - CCD readout to buffer 4:1 at 180KHz
  - 2 readout channels per CCD
  - ADC must be 14-"good bits"
  - Therefore, 16-bit ADC needed
  - Summing 4 16-bit ADCs,
  - Therefore, 18-bit register needed
- **SWIR Drivers**
  - 69 Fibers
- **Processor Drivers**
  - Increased Data Volume and no On-board Processing
  - Change from Coldfire (OCE-v2 study) to BAE 750 (OCE-v3)

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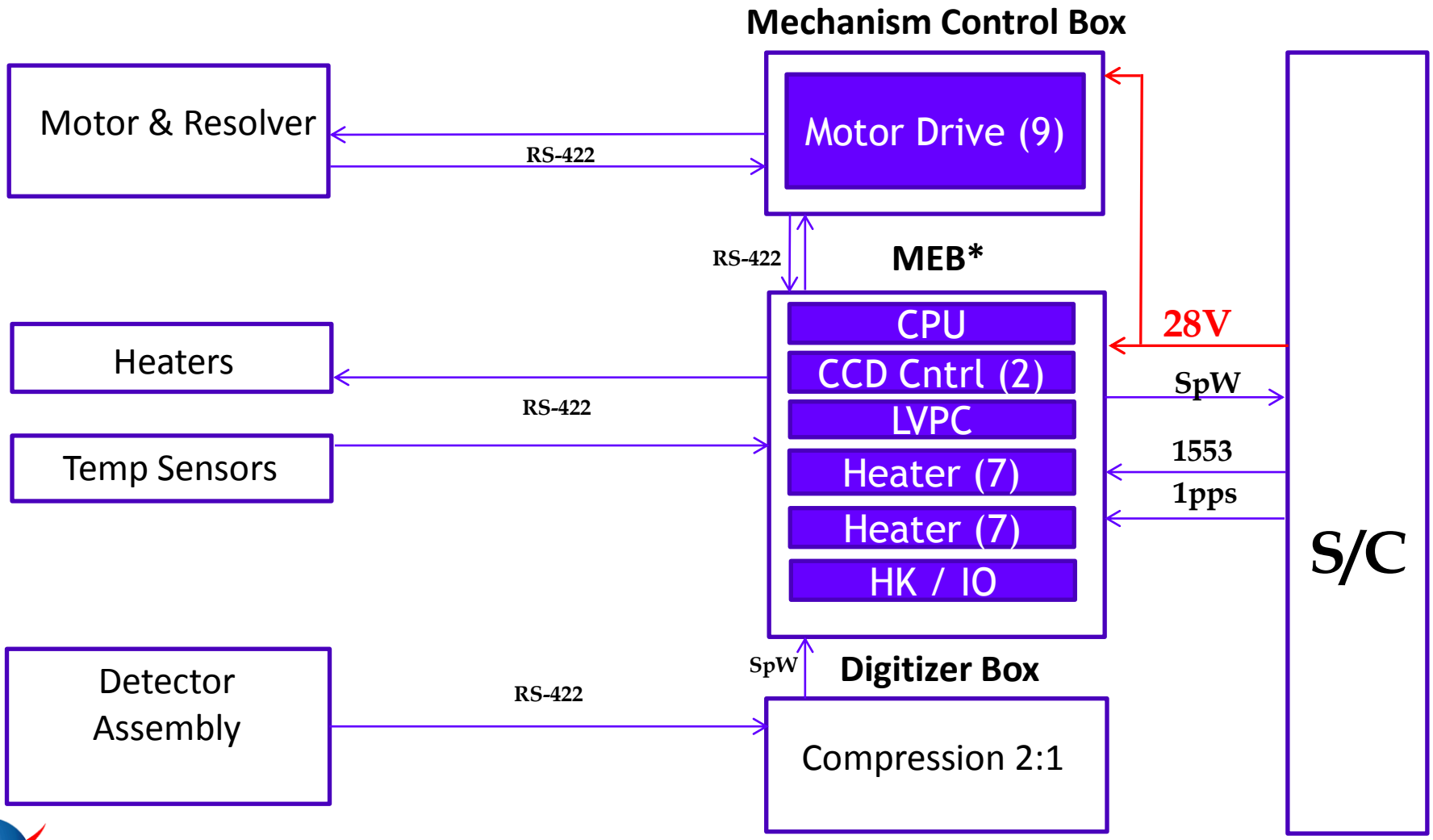
Electrical Boxes Block Diagram



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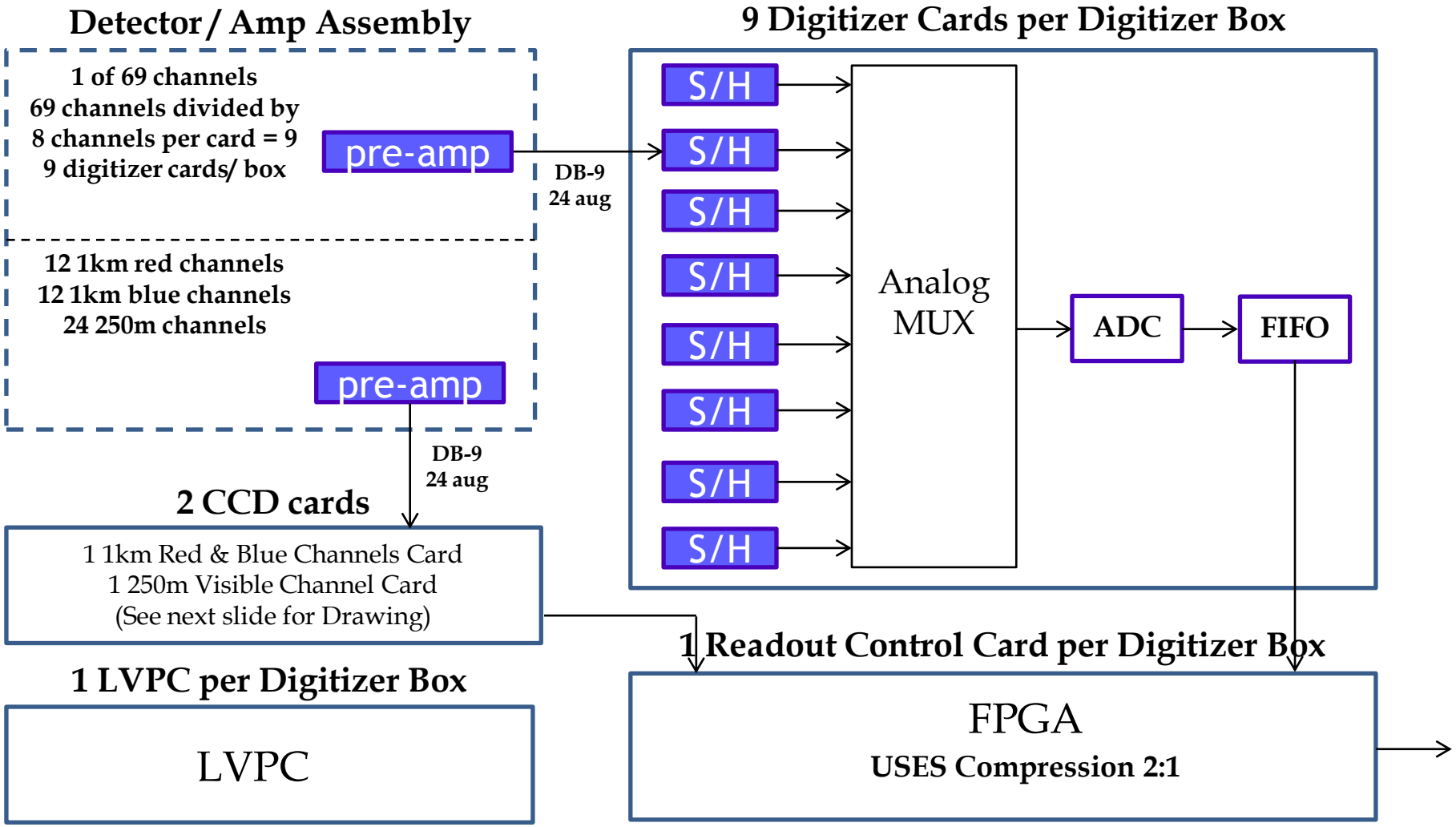
Digitizer Electronics



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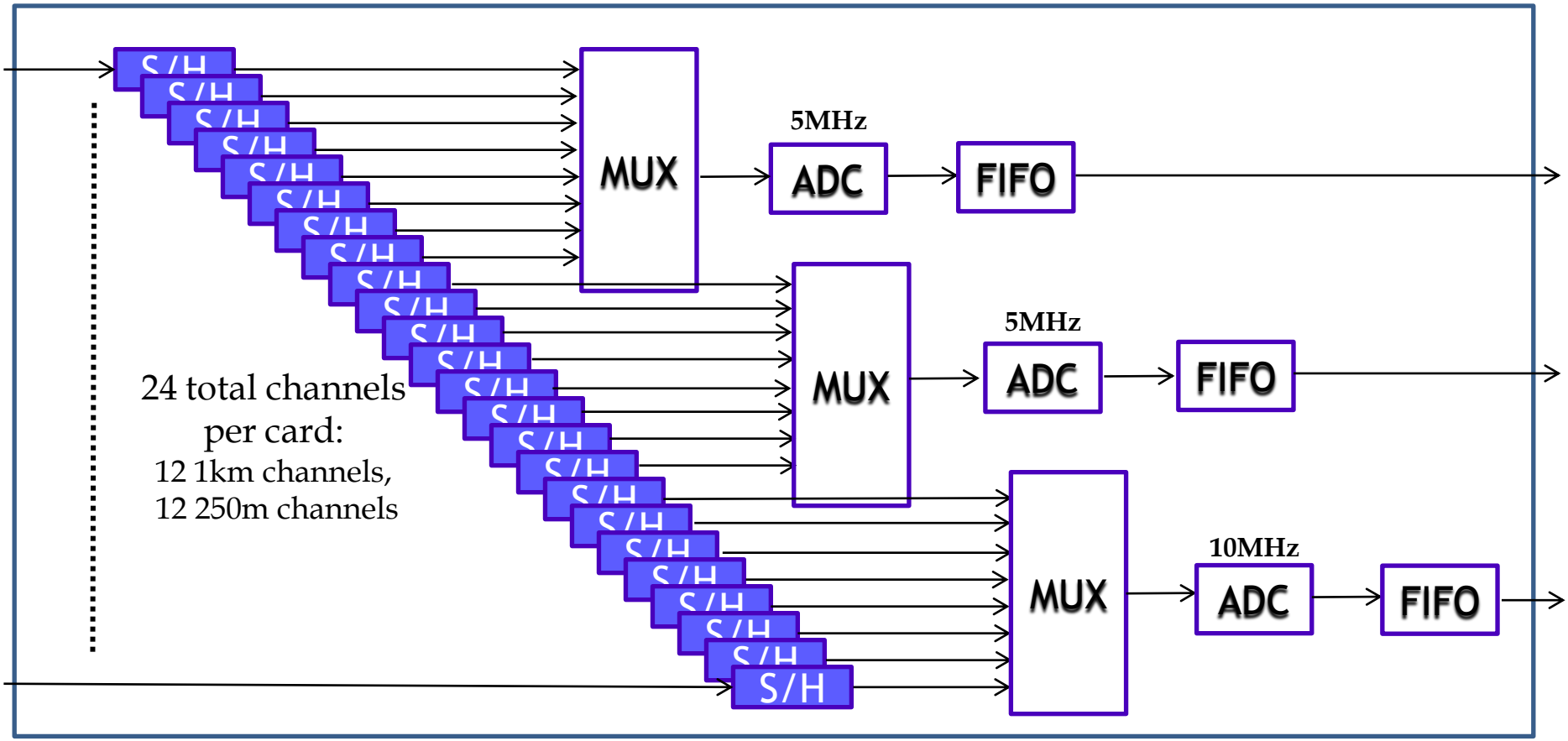
CCD Card



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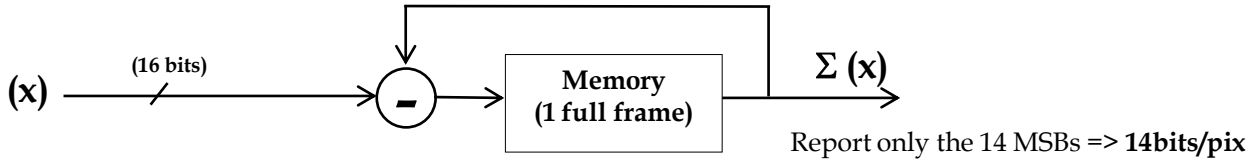
Correlated Double Sampling (CDS) Logic

Pixel CDS Algorithm



Report only the 14 MSBs => **14bits/pix**

Correlated Double Sampling
Readout and store entire frame (pixels) at beginning of integration period, then readout entire frame at end of integration period, then subtract initial frame from final frame to produce a CDS frame.

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Mechanism Electronics

Baseline:

- Board-size is 6u
- Redundant windings and mechanism control for the scanning mechanism (not cross-strapped)
- Redundant mechanism control for the scanning mechanism (not cross-strapped)
- Redundant operational and survival heaters, thermostats, and control circuits

Mechanism Box

- Scanning Mechanism
- Scanning Mechanism redundant
- Half-angle Mirror Mechanism
- Half-angle Mirror Mechanism redundant
- Momentum Compensation Mechanism
- Momentum Compensation Mechanism redundant
- Tilt Mechanism Motors 1
- Tilt Mechanism Motors 2
- Sun Calibration Mechanism

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MEB Power

E-Box External Load	Power (W)
Detector and Amp Dissipation	69.0
Motors/Actuators	38.3
Mechanism Control	15.0
E-Box External Dissipation:	**122.3**
E-Box Boards	**Power (W)**
CPU Board	15.0
HK	2.0
Thermal Control (2)	28.0
CCD Driver Boards (2)	20.0
E-Box Boards Dissipation:	**65.0**
E-Box Power Board Load	187.3
Converter % Efficiency	75
E-Box Converter Dissipation:	**62.4**
E-Box Dissipation:	**127.4**

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Mechanisms Box Power

- **Motors/Actuators:**
  - Scan Tel (14 W avg),
  - HAM (4.3 W avg),
  - Mom Comp (20 W avg)
- **Total:**
  - 38.3 W

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Digitizer Box Power

E-Box Boards	Power (W)
Digitizer Card Fiber (9)	45.0
CCD (2)l	19.0
Readout (1)	5.0
E-Box Boards Dissipation:	**69.0**
E-Box Power Board Load	69.0
Converter % Efficiency	75
E-Box Converter Dissipation:	**23.0**
E-Box Dissipation:	**92.0**

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Digitizer Box Power Calculations

- **Digitizer**
  - Sample n Hold = 135mW x 8 = **1080mW** (intersil HS-2420RH)
  - MUX = .01uW x 1 = **.01uW**
  - ADC = 1.5W x 1 = **1.5W** (Texas Instruments ADS8422) (4Msps)
  - FIFO = 2.5W x 1 = **2.5W** (Honeywell HX6409/HX6218/HHX6136)
  - Total per Digitizer Card = **5W per card**
  - 9 Digitizing Cards per box
- **CCD**
  - Sample n Hold = 135mW x 8 = **1080mW** (intersil HS-2420RH)
  - MUX = .01uW x 3 = **.03uW**
  - ADC 5MHz = 18mW x 2 = **36mW** (Texas Instruments ADS8319) (5Msps)
  - ADC 10MHz = 960mW x 1 = **960mW** (Texas Instruments ADS1610) (10Msps)
  - FIFO = 2.5W x 3 = **7.5W**
  - Total per CCD Card = **9.5W** per card
  - 2 CCD Cards per box
- **1 Readout Card**
  - FPGA & Memory = **5W**
- **1 LVPC Dissipation = 23W**
- **Total per box = 92W**
- **Total Digitizing Power = 92W**

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MEB Size

			Comments
Length	**Width**	**Quantity**	
9	*6*	*7*	Length/Width in inches
22.86	15.24		Length/Width in centimeters (1in = 2.54 cm)
Backplane:			
9	5	0.4	Backplane Length/Width in inches, Mass in Kg.
Board Mass Total:	*5.74 Kg*		My Metric: 0.5 Kg each 8"x6" board
	12.6 lbs		1lb = 0.45359237 Kg, 1Kg =2.204Kg
			1 in = 0.0254 meters = 2.54cm = 25.4 mm, 1 meter = 39.370 in

Electronics Box			
Depth (D)	**Height (H)**	**Width (W)**	
10	*7*	*8*	
25.4	17.78	20.32	(centimeters). Divide by 100 for meters
Surface Area Total	0.27		Area = 2(DH+HW+WD)/10000 square meters
Wall thickness (mm)	2.50		millimeters. Divide by 1000 for meters
Density (Aluminum)	2,700.00		Kg/Meter3
Housing Mass:	1.5 Kg		(Mass = Volume x Density. ie Area x Thickness x Density)
	3.3 lbs		
Box Mass Total:	7.24 Kg		(ie. C8+C19)
	15.9 lbs		(ie. C9+C20)

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Digitizer Box Size

Length	Width	Quantity	Comments
9	*6*	13	Length/Width in inches
22.86	15.24		Length/Width in centimeters (1in = 2.54 cm)
Backplane:			
9	13	1.2	Backplane Length/Width in inches, Mass in Kg.
Board Mass Total:	*8.5 Kg*		My Metric: 0.5 Kg each 8"x6" board
	18.8 lbs		1lb = 0.45359237 Kg, 1Kg =2.204Kg
			1 in = 0.0254 meters = 2.54cm = 25.4 mm, 1 meter = 39.370 in

Electronics Box			
Depth (D)	**Height (H)**	**Width (W)**	
10	*7*	*14*	
25.4	17.78	35.56	(centimeters). Divide by 100 for meters
Surface Area Total	0.40		Area = 2(DH+HW+WD)/10000 square meters
Wall thickness (mm)	2.50		millimeters. Divide by 1000 for meters
Density (Aluminum)	2,700.00		Kg/Meter3
Housing Mass:	2.7 Kg		(Mass = Volume x Density. ie Area x Thickness x Density)
	5.9 lbs		
Box Mass Total:	11.2 Kg		(ie. C8+C19)
	24.7 lbs		(ie. C9+C20)

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Mechanisms Box Size

Length	Width	Quantity	Comments
8	*7*	*10*	Length/Width in inches
20.32	17.78		Length/Width in centimeters (1in = 2.54 cm)
Backplane:			
8	10	0.8	Backplane Length/Width in inches, Mass in Kg.
Board Mass Total:	*6.7 Kg*		My Metric: 0.5 Kg each 8"x6" board
	14.7 lbs		1lb = 0.45359237 Kg, 1Kg =2.204Kg
			1 in = 0.0254 meters = 2.54cm = 25.4 mm, 1 meter = 39.370 in

Electronics Box			
Depth (D)	**Height (H)**	**Width (W)**	
9	*8*	*11*	
22.86	20.32	27.94	(centimeters). Divide by 100 for meters
Surface Area Total	0.33		Area = 2(DH+HW+WD)/10000 square meters
Wall thickness (mm)	2.50		millimeters. Divide by 1000 for meters
Density (Aluminum)	2,700.00		Kg/Meter3
Housing Mass:	2.1 Kg		(Mass = Volume x Density. ie Area x Thickness x Density)
	4.6 lbs		
Box Mass Total:	8.7 Kg		(ie. C8+C19)
	19.1 lbs		(ie. C9+C20)

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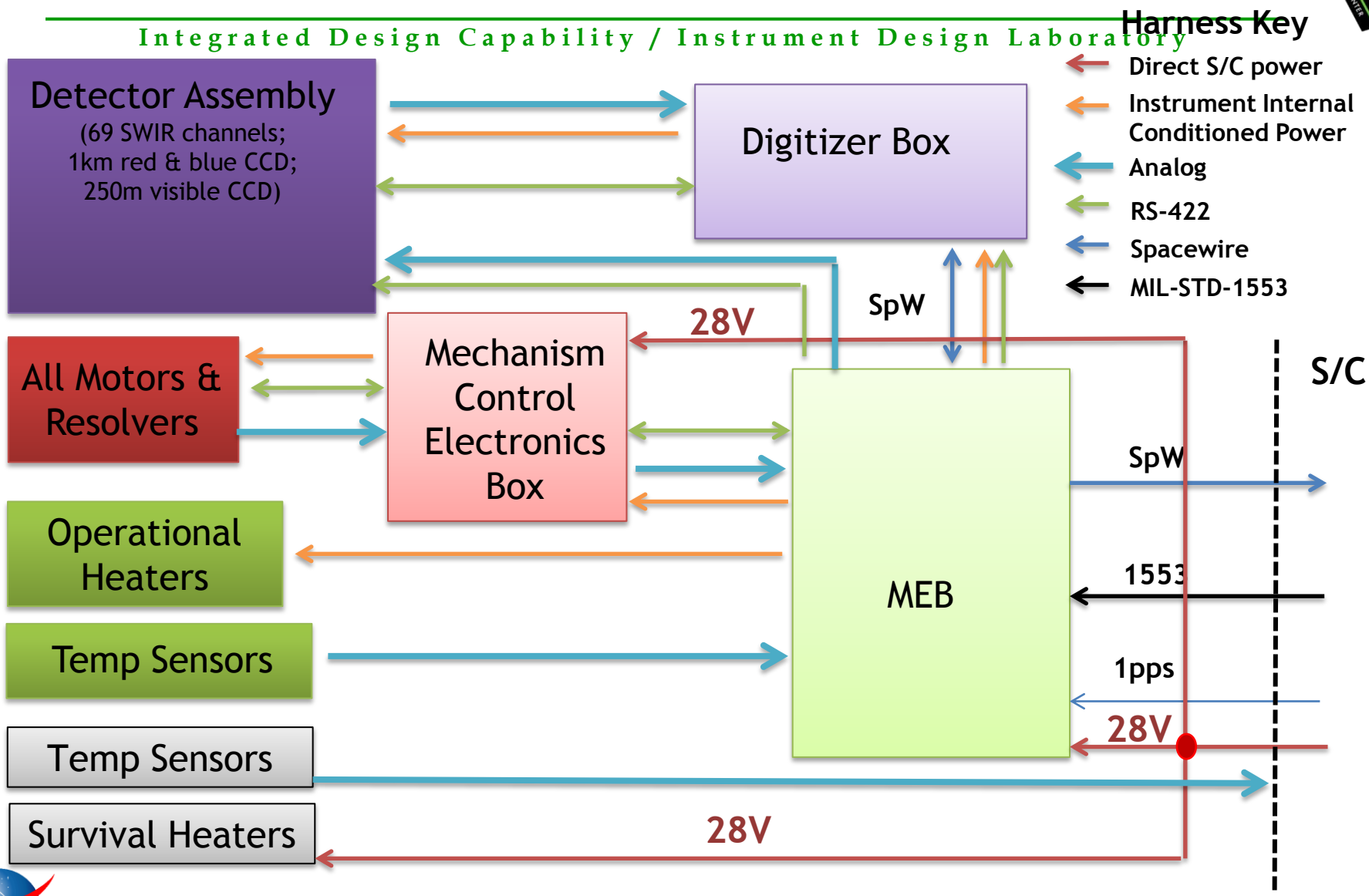
Electrical Interfaces



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Electrical Board Functionality

- **MEB**
  - CPU: Central Processing Unit-
    - Reads the buffered data from HK/IO Card, packetizes it w CCSDS headers and timestamp, sends to Spacecraft
    - Receives commands coming from Spacecraft via 1553
  - HK/IO: Housekeeping and Input Output
    - Reads thermistors
    - Buffers Digitizer Data from Digitizer Box going to CPU
  - Heater Card (2: 1 primary, 1 redundant):
    - 7 thermal control circuits per card
  - LVPC: Low Voltage Power Converter
    - Steps-down Spacecraft power to regulated power needed for MEB
  - CCD Control Board (2)
- **Digitizer Box**
  - Digitizer Cards for fibers
    - Digitize the signals
  - CCD Card
    - Digitize the signals
  - Readout Board
    - Compress data
    - Buffer data to send to MEB via SpW

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Electrical Board Functionality

- **Mechanisms Box**
  - Scanning Mechanism (2: 1 primary, 1 redundant)
    - Controls angular position vs time of the scan tube mirror to within + or – 15 arcsecs of the nominal position, set by precision clock
    - Output pulse to data acquisition to trigger integration time for each pixel
  - Half-angle Mirror Mechanism (2: 1 primary, 1 redundant)
    - Controls the angular position vs time of the half-angle mirror to within + or – 15 arcsecs of the scan tube position
  - Momentum Compensation Mechanism (2: 1 primary, 1 redundant)
    - Hold the speed of the momentum compensator wheel nominally correct to cancel angular momentum of the scan tube
  - Tilt Mechanism (2)
    - Rotates the stepper motors 180deg to control the tilt of the scan tube
  - Sun Calibration
    - Rotates the calibration targets 120deg on command, which controls the rotation of the shaft
  - LVPC: Low Voltage Power Converter
    - Steps-down Spacecraft power to regulated power needed for Mechanisms Box

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Electrical Board Size and Count

- **Board Size**
  - All boards are 6u size (230mm x 160mm)
- **Board Count per Box**
  - 7 cards in MEB (2 CCD Control cards out of the total 7)
  - 13 cards in Digitizer Box
  - 9 cards in Mechanisms Box

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Electrical Redundancy

- **MEB:**
  - Redundant Thermal Control Card
- **Mechanisms**
  - Redundant windings and mechanism control for the scan tube mechanism (not cross-strapped)
  - Redundant mechanism control for the momentum compensator mechanism (not cross-strapped)
  - Redundant operational and survival heaters, thermostats, and control circuits
  - Redundant boards for HAM, scan, and MOM

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OCE v3 Harness Mass Estimates *have been refined for higher fidelity since OCE v2

Harness ID		Harness Parameters						Connector & Backshell		Total
Source (From)	Destination (To)	Type (Select)	Description (Table Lookup)	Qty	Length (m)	Density (g/m)	Mass (g)	Type (Select)	(x2) Mass (g)	Mass (g)
Digitizer Box	CCDs	TSP-24AWG	M27500-24SC2S23	45	1.0	18.37	826.77	62P (HD)	89.60	916.37
Digitizer Box	Photo Diodes	TSP-24AWG	M27500-24SC2S23	69	1.0	18.37	1267.72	78P (HD)	95.60	1363.32
MEB	Digitizer Box	RS422	5 wires (2 TSPs + GND)	1	0.3	39.99	10.00	15P (LD)	48.00	58.00
MEB	Digitizer Box	Power	Twisted Pair (12AWG)	1	0.3	69.55	20.87	(Shared)	0.00	20.87
MEB	MCEB	RS422	5 wires (2 TSPs + GND)	1	0.5	39.99	20.00	15P (LD)	48.00	68.00
MEB	MCEB	Power	Twisted Pair (12AWG)	1	0.5	69.55	34.78	(Shared)	0.00	34.78
MEB	Operational Heaters	TP-24AWG	M27500-24SC2U00	14	2.5	7.22	252.62	25P (LD)	62.40	315.02
MEB	Temperature Sensors	TSP-24AWG	M27500-24SC2S23	14	2.5	18.37	643.04	25P (LD)	62.40	705.44
MEB	CCDs	TSP-24AWG	M27500-24SC2S23	3	1.0	18.37	55.12	9P (LD)	39.60	94.72
MEB	Digitizer Box	SpaceWire	9 wires (4 TSPs + GND)	3	0.3	74.80	67.32	9P (LD)	39.60	106.92
MCEB	Scan Motor	Power	Twisted Pair (12AWG)	16	1.6	69.55	1780.58	21P (MDM)	33.20	1813.78
MCEB	Scan Motor Resolver	LVDS	26453/9N173X-2 (LD)	12	1.6	13.78	264.57	(Shared)	0.00	264.57
MCEB	HAM Motor	Power	Twisted Pair (12AWG)	16	1.4	69.55	1558.01	21P (MDM)	33.20	1591.21
MCEB	HAM Motor Resolver	LVDS	26453/9N173X-2 (LD)	12	1.4	13.78	231.50	(Shared)	0.00	231.50
MCEB	Comp. Motor	Power	Twisted Pair (12AWG)	16	1.6	69.55	1780.58	21P (MDM)	33.20	1813.78
MCEB	Comp. Motor Resolver	LVDS	26453/9N173X-2 (LD)	12	1.6	13.78	264.57	(Shared)	0.00	264.57
MCEB	Tilt Motor	Power	Twisted Pair (12AWG)	6	1.4	69.55	584.25	21P (MDM)	33.20	617.45
MCEB	Tilt Motor Encoder	LVDS	26453/9N173X-2 (LD)	6	1.4	13.78	115.75	(Shared)	0.00	115.75
MCEB	Cal. Motor	Power	Twisted Pair (12AWG)	6	1.0	69.55	417.32	21P (MDM)	33.20	450.52
MCEB	Cal. Motor Encoder	LVDS	26453/9N173X-2 (LD)	6	1.0	13.78	82.68	(Shared)	0.00	82.68
		-	-			0.00	0.00	-	0.00	0.00
						Total:	**10278.03**		**651.20**	10929.23g
									Total:	**10.93Kg**
									+ 5% misc :	**11.48Kg**

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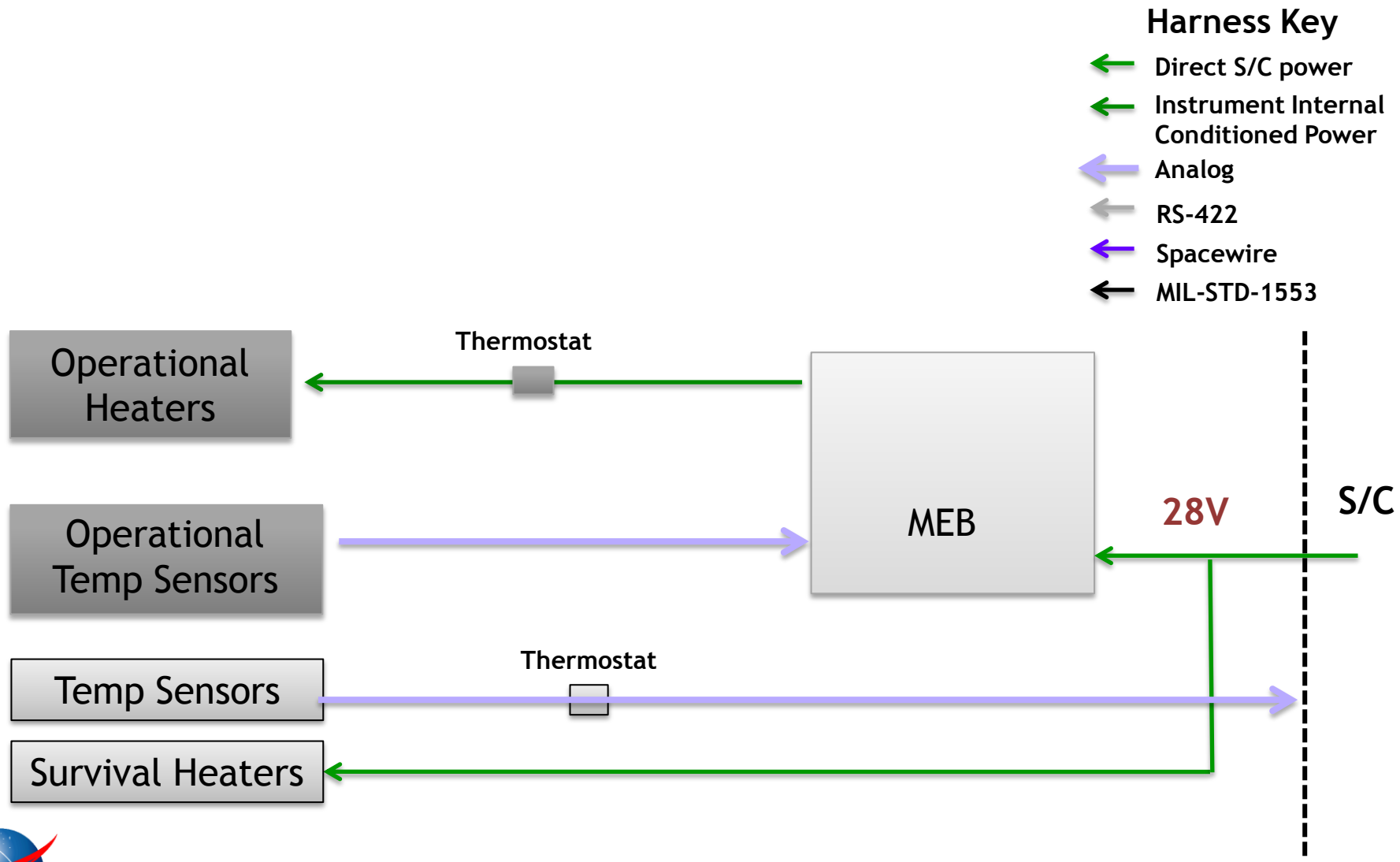
Thermal Harness



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Technology Needs

- **16-bit rad-hard ADC @ 10MHz**
  - One selected may need to be qualified

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Risk/Concerns

- N/A

* Add Extra board for CCD Cntrl to MEB

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Conclusions

- **3 electrical boxes**
  - MEB:
    - (unchanged from OCE v2 save CPU: Coldfire to BAE Rad750),
  - Mechanisms Box (unchanged)
  - Digitizer Box, changes as follows:
    - 9 SWIR boards
    - 2 CCD boards

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Future Recommendations

- **Split Digitizer Box into 2 boxes for I&T purposes?**
  - CCDs in 1 box, Dig Cards in 1 box
  - Would add mass

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Backup Charts

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Predefined Schema for Costing New FPGA Developments

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FPGA Firmware Development Costs

- **Predefined schema for costing Field Programmable Gate Array (FPGA) firmware development**
  - Our parametric cost estimate includes the procurement costs for flight FPGAs hardware chip set(s)
  - We use this scheme to capture the NRE costs for the engineering labor to generate and test the algorithms for spaceflight
  - The resulting estimate is general and coarse and should be refined as the instrument matures, but we feel it serves as a reasonable placeholder to our customers
- **Many functions and algorithms that have been previously designed and coded, and are available as intellectual Property (IP) in VHDL Format**
  - We assume that other NASA centers and vendors would also have heritage algorithms to take advantage of in their spaceflight programs
  - Although their experience may differ from Goddard's we feel that they would likely have the same overall ratio of new to heritage algorithms
  - IP developed by NASA is assumed to be available for free
  - IP provided by industry requires a license for its usage
- **Our costing scheme**
  - Historically it has required very little FTEs to implement heritage VHDL IP into an FPGA, and that
  - We estimate that heritage algorithms can be implemented for free, and that new algorithms require $400k of development labor
  - We assume each new FGPA chip, even if it includes all heritage algorithms, requires $400k of development labor to establish the external interfaces and layout the basic chip architecture
  - Copies of identical FPGA chips are assumed to be free

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Heritage Firmware

- **Examples of VHDL IP that are available to GSFC teams**
  - Spacewire Data Network Protocol/interface
  - PCI Data Bus Interface for both Bus Controller and Terminals
  - Mil-STD-1553 Data Bus Controller and Remote Terminals
  - Short Reed-Solomon Encoder/Decoder for Error Detection & Correction (EDAC) of Data in SEU vulnerable memory
  - Rice Data Compression Algorithm (~2:1 Lossless)
  - Pixel-Processor (for science data reduction)
  - Downlink Formatting & Encoding
    - CCSDS VCDU protocol Formatting
    - Long Reed-Solomon Encoding for EDAC across downlink channels
    - Convolution Encoding
    - Randomization
- **The most used FPGA on future missions is the Actel AX-2000, but this scheme is independent of the hardware implementation**
  - We try to evaluate the chip capacity as we identify the number of req'd FPGAs in the electrical architecture, but this should also be confirmed as the instrument concept matures

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FPGA Firmware Costing Scheme

- **Originally documented in 2007, this scheme was revised by several Product Design Leads (PDLs) in Code 564 in Oct, 2011 for the IDL to capture the firmware development labor associated with FPGAs**
  - We do not have any insight into the labor expended by other Centers or Vendors to develop FPGA firmware, so if an out-of-house build is assumed, this estimate should be considered a reasonable placeholder
  - The hardware costs are captured parametrically
- **$400K Minimum for FPGA Development for the chip pin assignments and interface frame work, for each unique FPGA (firmware costs are assumed to be zero for identical FPGA chips)**
  - 1.50 FTEs of New Code Design (VHDL coding and Simulation)
  - 0.50 FTEs of New Code Verification (by Analysis)
  - 0.25 FTEs of Signal Integrity Analysis (of all I/O lines)
  - 0.25 FTEs of Lab Code Test
- **$400K per unique Algorithm, which are executed from within the FPGA frame work**
  - 1.00 FTEs of New Algorithm
  - 1.00 FTEs of New Algorithm lab Test/Verification

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